REMARKS

Reconsideration of the above identified application in view of the preceding amendments and following remarks is respectfully requested. Claims 1, 3-8 and 10-15 are pending in this application. By this Amendment, Applicants have amended Claims 1, 8 and 15.

In the outstanding Office Action, Claims 1, 8 and 15 were rejected under 35 U.S.C. § 103 (a) over U.S. Patent Application No. 2004/0036708 to Evanicky et al. in view of U.S. Patent No. 6,219,040 to Kotha et al.

Evanicky et al. show a computer system having a graphics subsystem in Figure 1. The graphic subsystem 19 is connected to an address/data bus for communicating information. The address/data bus also allows communication with ROM 13, RAM 14, and a data storage device 15. Figure 10 and the associated description at paragraph 71 provide elaboration on the function of the graphics subsystem (referred to therein by reference numeral 18). The graphics subsystem includes a graphics constroller 730. The graphics controller receives input signal image data and control signals and converts the image data to appropriate RGB values using graphics rendering engines. The graphics subsystem also includes a frame rate modulator that receives a video signal generated by the graphics controller. The frame rate modulator is used for generating an intermediate gray-scale value by rapidly alternating between meighboring gray-scale values in a cathode ray tube display.

Kotha et al. describes a frame rate modulation block configured to repeat or skip selected numbers of adjacent frames in a video signal in order to provide a proper refresh rate for a flat panel display (see col. 7, lines 46-52). Kotha et al. discloses nothing more of any relevance to the subject claims.

It is plain from the discussion above that Evanicky et al. in view of Kotha et al. do not teach or suggest, either in whole or in part, alone or together, the subject claims. In particular, the signal processing unit defined by Claim 1 recites a first device which acts on a video signal by overlaying graphical picture elements and text characters onto an input video signal to produce a first device output video signal; a second device which converts a frame rate of the first device output video signal to produce an increased frame rate video signal; a picture storage device accessed by the first and second devices during processing of the video signal and first device output video signal, respectively, for storing and retrieving picture data for the first and second devices; and a driver stage which drives a display responsive to the increased frame rate video signal. The combination of references do not disclose or suggest such a structural configuration. For example, the graphics controller of Evanicky et al. does not overlay graphical picture elements and text characters on the input video signal. The frame rate modulator of Evanicky et al. does not increase the frame rate, rather it modulates the frame rate. Moreover, the graphics controller and frame rate modulator of Evanicky et al. do not access a common picture storage device. Evanicky et al. merely describes that the graphics controller only receives image data from a processor of the computer system. The graphics controller of Evanicky et al. does not access a picture storage device, the ROM 13 or RAM 14. The frame rate modulator of Evanicky et al. only receives an input signal from the graphics controller, i.e. it is not capable of accessing any of the components connected to the

address/data bus shown in Figure 1. Further, the graphics system of Evanicky et al. only receives image data from the address/data bus. There is no teaching in Evanicky et al. of having the graphics system transmit any data to the address/data bus as denoted by the direction of the arrows in Figure 10. Consequently, Claim 1 and each of the remaining claims depending therefrom are not rendered obvious by the reference cited by the Examiner, and withdrawal of the rejection under 35 U.S.C. §103(a) is respectfully requested.

Similarly, Claim 15 recites a signal processing unit for a digital TV system, including a common storage device for storing and retrieving picture data; a first device for acting on an input video signal by overlaying graphical picture elements and text characters to produce a processed video signal, wherein the first device stores and retrieves picture data from the common storage device; and a second device for increasing a frame rate of the processed video signal, wherein the second device stores and retrieves picture data from the common storage device. It is black letter law that it is impermissible for the Examiner to read teachings into references which are simply not there and such structure is not present in the cited references even if combined. Consequently, Claim 15 is not rendered obvious by the reference cited by the Examiner, and withdrawal of the rejection under 35 U.S.C. §103(a) is respectfully requested.

Turning to Claim 8, it recites, *inter alia*, a method for processing a digital TV system signal, including acting by a first device on an input video signal by overlaying graphical picture elements and text characters to produce a processed video signal, wherein the first device stores and retrieves picture data from a common storage device; and increasing by a second device the frame rate of the processed video signal to produce an increased frame rate video signal, wherein the second device stores and retrieves picture

data from the common storage device. The combination of references do not disclose or suggest such method steps. Consequently, Claim 8 and each of the remaining claims depending therefrom are not rendered obvious by the reference cited by the Examiner, and withdrawal of the rejection under 35 U.S.C. §103(a) is respectfully requested.

In the outstanding Office Action, Claims 3-7 and 10-14 were rejected under 35 U.S.C. § 103 (a) over U.S. Patent Application No. 2004/0036708 to Evanicky et al. in view of U.S. Patent No. 6,219,040 to Kotha et al. and further in view of U.S. Patent No. 6,549,240 to Reitmeier.

Reitmeier simply uses a frame buffer to increase the frame rate without allowing the memory components to be accessed by any other component for any other purpose.

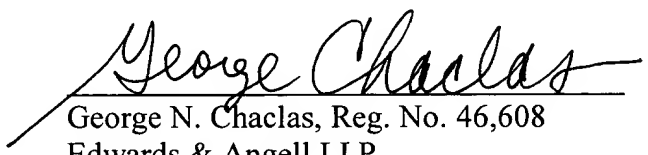
It is respectfully submitted that Reitmeier does not cure the deficiencies noted above with respect to Claims 1, 8 and 15. Therefore, each claim depending therefrom is not rendered obvious by the reference cited by the Examiner, and withdrawal of the rejection under 35 U.S.C. §103(a) is respectfully requested.

Any additional fees or overpayments due as a result of filing the present paper may be applied to Deposit Account No. 04-1105. It is respectfully submitted that all of the claims now remaining in this application are in condition for allowance, and such action is earnestly solicited.

If after reviewing this amendment, the Examiner believes that a telephone interview would facilitate the resolution of any remaining matters the undersigned attorney may be contacted at the number set forth herein below.

Respectfully submitted,

Date: October 12, 2005



George N. Chaclas, Reg. No. 46,608
Edwards & Angell LLP
Attorney for Applicants
P.O. Box 55874
Boston, MA 02205-5874
Tel: (401) 276-6653
Fax: (888) 325-1684